

CLAIMS

What is claimed is:

1. A chip carrier, comprising:

a first side;

a second side opposing the first side and removed finally from an engaged surface of a mold in a de-molding process; and

at least one grounding means formed on the second side corresponding in position to an eject pin of the mold.

2. The chip carrier of claim 1, further comprising:

a base layer having a first surface and a second surface opposing the first surface;

a plurality of conductive traces disposed on the first surface of the base layer and electrically connected to a semiconductor chip;

a plurality of ball pads formed on the second surface of the base layer for implanting a plurality of solder balls thereon;

a plurality of vias for electrically connecting the conductive traces to the ball pads respectively;

a die pad formed on the first surface of the base layer for mounting the semiconductor chip thereon; and

a solder mask layer deposited on each of the first and second surfaces of the base layer in a manner that part of the conductive traces electrically connected to the semiconductor chip on the first surface and the ball pads on the second surface are respectively exposed to outside of the solder mask layer.

3. The chip carrier of claim 1, wherein the grounding means is formed by plating a conductive material.
4. The chip carrier of claim 3, wherein the conductive material is gold.
5. The chip carrier of claim 2, wherein the grounding means is exposed to the outside of the solder mask layer.
6. The chip carrier of claim 2, wherein the grounding means is electrically connected to a grounding trace disposed on the first side of the chip carrier by a grounding via formed through the base layer.
7. A semiconductor package, comprising:
 - a chip carrier having a first side and a second side opposing the first side;
 - at least one semiconductor chip mounted on the first side of the chip carrier;
 - a plurality of conductive elements for electrically connecting the semiconductor chip to the chip carrier:
 - an encapsulant formed of a molding compound for encapsulating the semiconductor chip and the conductive elements on the first side of the chip carrier; and
 - a plurality of solder balls implanted on the second side of the chip carrier;
 - wherein on one of the sides of the chip carrier finally removed from an engaged surface of a mold in a de-molding process there is formed at least one grounding means corresponding in position to an eject pin of the mold.
8. The semiconductor package of claim 7, wherein the chip carrier further comprises:
 - a base layer having a first surface and a second surface opposing the first surface;
 - a plurality of conductive traces disposed on the first surface of the base layer and electrically connected to the semiconductor chip;

a plurality of ball pads formed on the second surface of the base layer for implanting the solder balls thereon;

a plurality of vias for electrically connecting the conductive traces to the ball pads respectively;

a die pad formed on the first surface of the base layer for mounting the semiconductor chip thereon; and

a solder mask layer deposited on each of the first and second surfaces of the base layer in a manner that part of the conductive traces electrically connected to the semiconductor chip on the first surface and the ball pads on the second surface are respectively exposed to outside of the solder mask layer.

9. The semiconductor package of claim 7, wherein the grounding means is formed by plating a conductive material.
10. The semiconductor package of claim 9, wherein the conductive material is gold.
11. The semiconductor package of claim 8, wherein the grounding means is exposed to the outside of the solder mask layer.
12. The semiconductor package of claim 8, wherein the grounding means is electrically connected to a grounding trace disposed on the first side of the chip carrier by a grounding via formed through the base layer.
13. A fabricating method of a semiconductor package, comprising:

preparing a chip carrier having a first side, and a second side opposing the first side and finally removed from an engaged surface of a mold in a de-molding process, wherein at least one grounding means is formed on the second side corresponding in position to an eject pin of the mold;

performing a die bonding process for mounting at least one semiconductor chip on the first side of the chip carrier;

providing a plurality of conductive elements for electrically connecting the semiconductor chip to the chip carrier;

performing a molding process for forming an encapsulant for encapsulating the semiconductor chip and the conductive elements on the first side of the chip carrier;

performing a de-molding process for ejecting the semi-fabricated semiconductor package from the mold by using the eject pins on the mold;

performing a ball implanting process for implanting a plurality of solder balls on the second side of the chip carrier; and

performing a singulating process for forming individual fabricated semiconductor packages.

14. The fabricating method of claim 13, wherein the chip carrier further comprises:

a base layer having a first surface and a second surface opposing the first surface;

a plurality of conductive traces disposed on the first surface of the base layer and electrically connected to the semiconductor chip;

a plurality of ball pads formed on the second surface of the base layer for implanting the solder balls thereon;

a plurality of vias for electrically connecting the conductive traces to the ball pads respectively;

a die pad formed on the first surface of the base layer for mounting the semiconductor chip thereon; and

a solder mask layer deposited on each of the first and second surfaces of the base layer in a manner that part of the conductive traces electrically connected to the semiconductor chip on the first surface and the ball pads on the second surface are respectively exposed to outside of the solder mask layer.

15. The fabricating method of claim 13, wherein the grounding means is formed by plating a conductive material.

16. The fabricating method of claim 15, wherein the conductive material is gold.

17. The fabricating method of claim 14, wherein the grounding means is exposed to the outside of the solder mask layer.

18. The fabricating method of claim 14, wherein the grounding means is electrically connected to a grounding trace disposed on the first side of the chip carrier by a grounding via formed through the base layer.

19. The chip carrier of claim 1, further comprising:

at least one grounding means formed on the first side of the chip carrier corresponding in position to the eject pin of the mold.

20. The semiconductor package of claim 7, wherein on one of the sides of the chip carrier not finally removed from the engaged surface of the mold in the de-molding process there is further formed at least one grounding means corresponding in position to the eject pin of the mold.

21. The fabricating method of claim 13, wherein the chip carrier further comprises:

at least one grounding means formed on the first side of the chip carrier corresponding in position to the eject pins of the mold.